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PG III

Paper/Unit- CC 12/I

Topic - used of 555 IC Timer

(A) Timer as Monostable Multivibrator

fig (2) is to be triggered externally

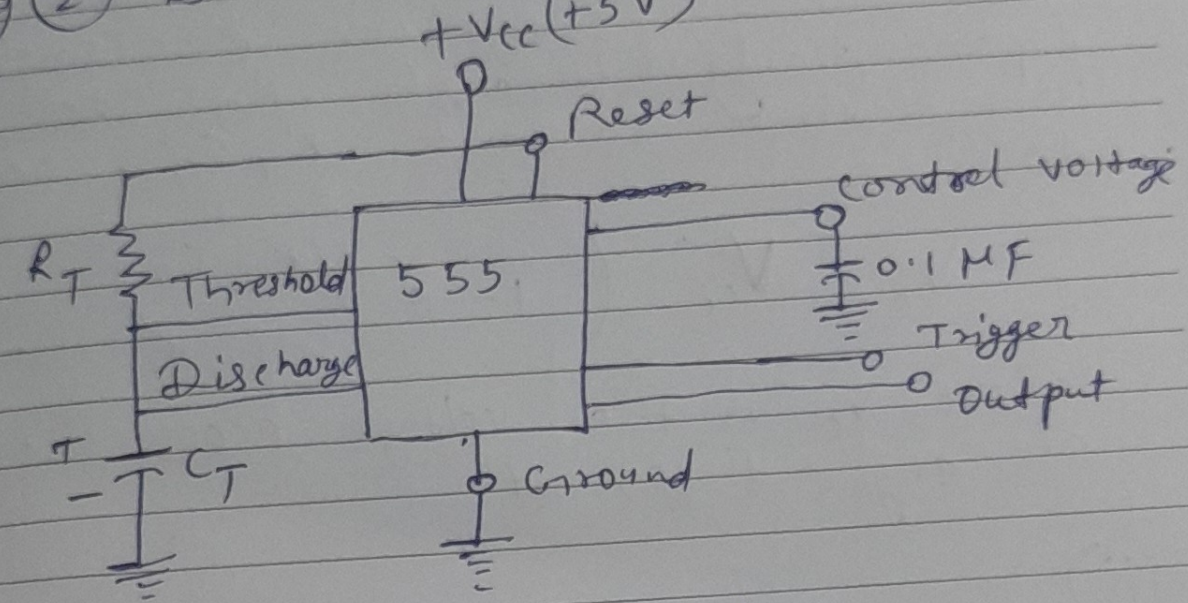


fig (2) 555 timer

for monostable mode of operation. We note that:

(i) When no trigger input is applied, capacitor C_T is held in the discharged state. In this state output is low.

(ii) When trigger input is applied and as the trigger voltage passes through $V_{CC}/3$ (threshold level of comp.-2), comparator-2 changes

its output state so that flip flop is set i.e $\bar{Q} = 0$ and transistor Q_1 becomes OFF. Hence timing cycle begins i.e capacitor C charges up exponentially through R_T towards V_{cc} with time constant $R_T C_T$, according to

$$V_c = V_{cc}\left(1 - e^{-t/R_T C_T}\right) \quad \text{— (1)}$$

where V_c is the voltage across the capacitor at any time, t.

(iii) when this voltage V_c, reaches $2V_{cc}/3$ (threshold level of comparator-1), as it is connected to threshold terminal, comparator-1 changes its output state so that flip flop is reset i.e

$\bar{Q} = 1$. This makes the transistor Q_1 ON and the capacitor discharges rapidly to ground; the timing cycle is completed. Once the circuit is triggered, it is insensitive to further triggering pulses until the timing cycle is completed.

(iv)

(iv) from points (ii) and (iii), we note that time period of the timing cycle is the time required for the capacitor to charge from zero to $2V_{cc}/3$. This period can be obtained on putting $V_c = 2V_{cc}/3$ at $t = T$ in eqn (1). That is

$$2V_{cc}/3 = V_{cc}\left(1 - e^{-T/R_T C_T}\right)$$

or $$T = R_T C_T \log_e \frac{V_{cc}}{V_{cc} - \frac{2}{3}V_{cc}}$$

$$\cong 1.1\, R_T C_T \quad — (2)$$

Thus pulse width is determined by external resistance & capacitance.

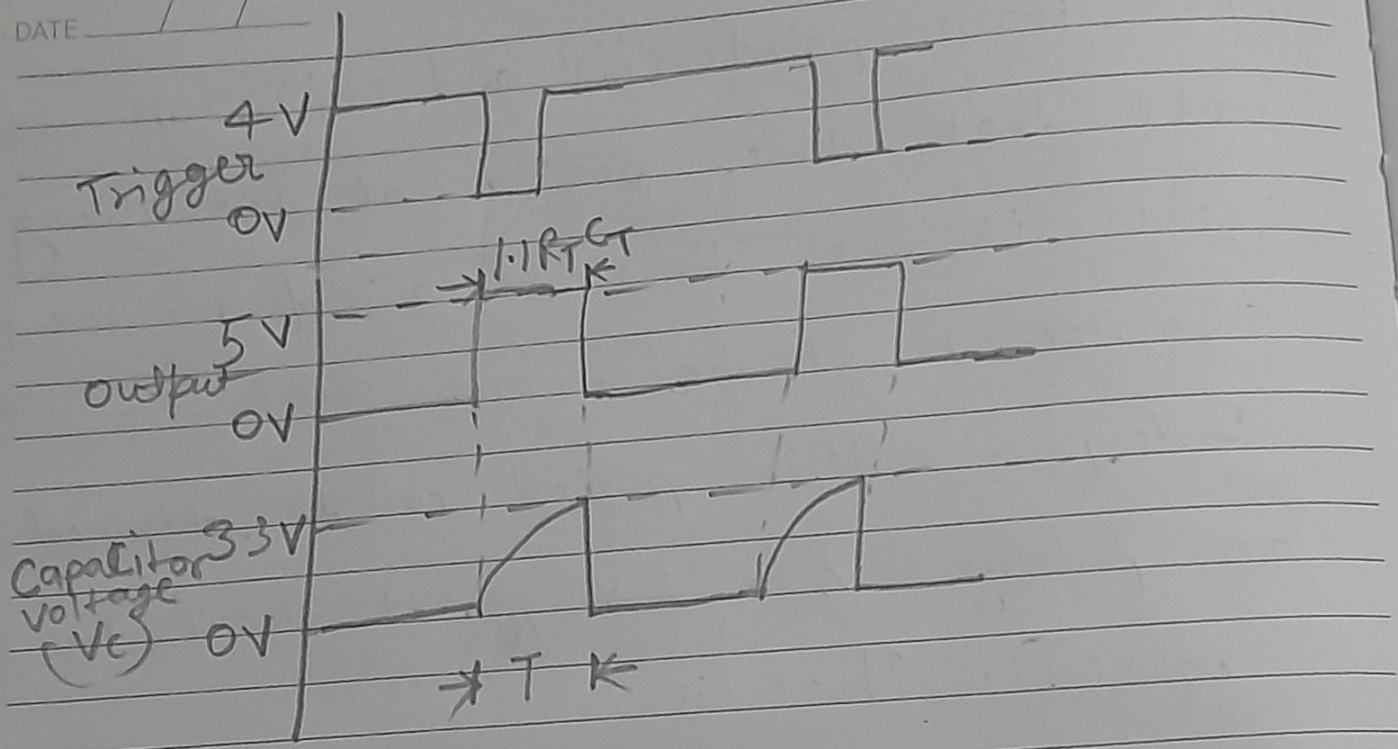


fig (3) 555 timer used as a one shot multivibrator.

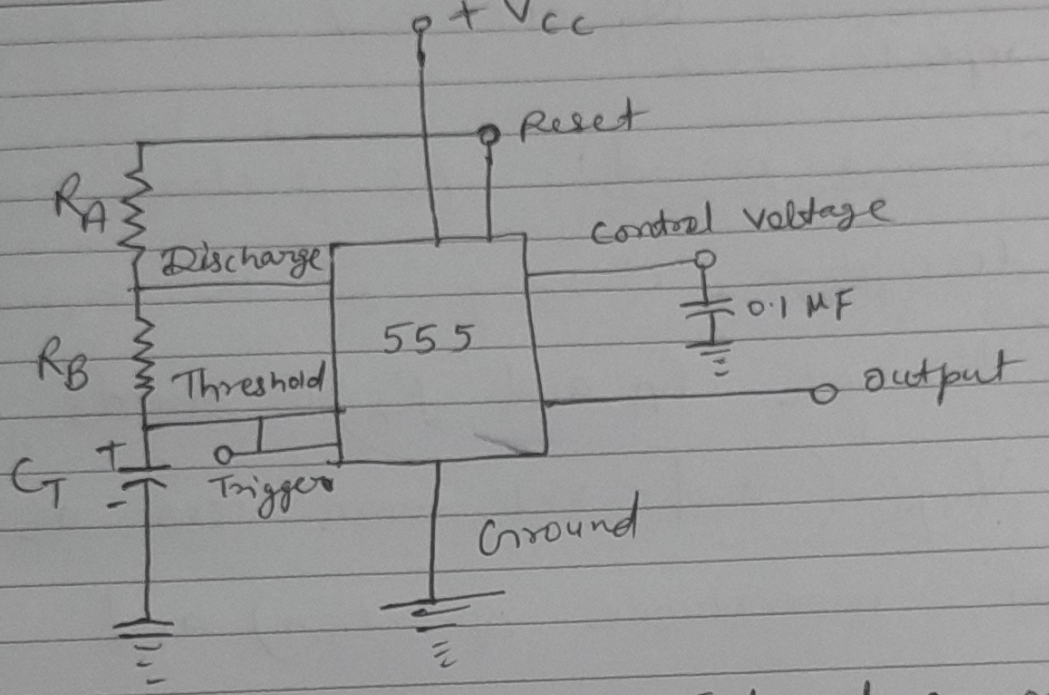
Note $V_c = 2\frac{V_{cc}}{3} = 2 \times \frac{5}{3} = 3.3\,V$

(B) Timer used as Astable multivibrator

External connections for astable operation are shown in fig (4). In this operation, circuit does not require any external trigger signal; therefore, trigger terminal is connected to threshold terminal so that at all time, V_c, is applied to both these inputs. Further two series resistors R_A and R_B are also used, whose common junction is connected

to discharge terminal. Its operation is as follows:

operation :-



fig④ 555 timer: External connections for astable operation.

During charging up period transistor Q_1 is held open by flip flop and capacitor charges through series connected resistors R_A and R_B. When voltage across capacitor reaches $2V_{cc}/3$ (reference level of comparator-1) comparator-1 changes its output state and it changes the state of flip flop so that transistor Q_1 is now ON. The capacitor then discharges through R_B until its

voltage drops to $V_{cc}/3$ (reference level of comparator 2). This comparator then changes the state of flip flop again which in turn makes the transistor Q_1 OFF and thus the cycle repeats itself.

Charging period:- As is clear from above description, charging of the capacitor (through R_A and R_B) starts from $V_{cc}/3$ (and not from zero as in case of monostable operation) and continues upto $2V_{cc}/3$.

Therefore eqn ② for this case becomes:

Charging period:

$$T_1 = C(R_A + R_B) \log_e \frac{V_{cc} - V_{cc}/3}{V_{cc} - 2V_{cc}/3}$$

$$= C(R_A + R_B) \log_e 2$$

$$= 0.7 (R_A + R_B) C$$

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Discharge period :- Capacitor discharges (through R_B only) from $2V_{cc}/3$ towards zero volt. This discharge is terminated at $V_{cc}/3$ at which comparator-2 changes state. Hence discharge period is determined by the eqn

$$T_2 = C R_B \log_e \frac{0 - 2V_{cc}/3}{0 - V_{cc}/3}$$

$$= 0.7 R_B C.$$

Total period : $T = T_1 + T_2$

$$= 0.7 (R_A + 2R_B) C)$$

charging and discharging intervals differ by $0.7 R_A C$.